

FIG. 1A
(PRIOR ART)

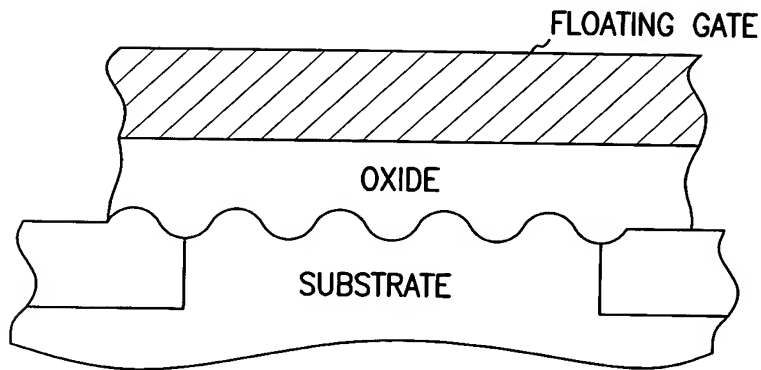


FIG. 1B
(PRIOR ART)

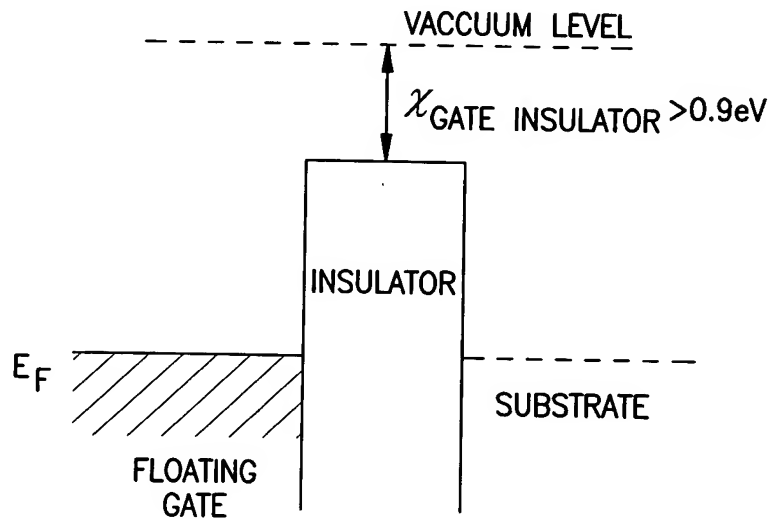


FIG. 1C
(PRIOR ART)

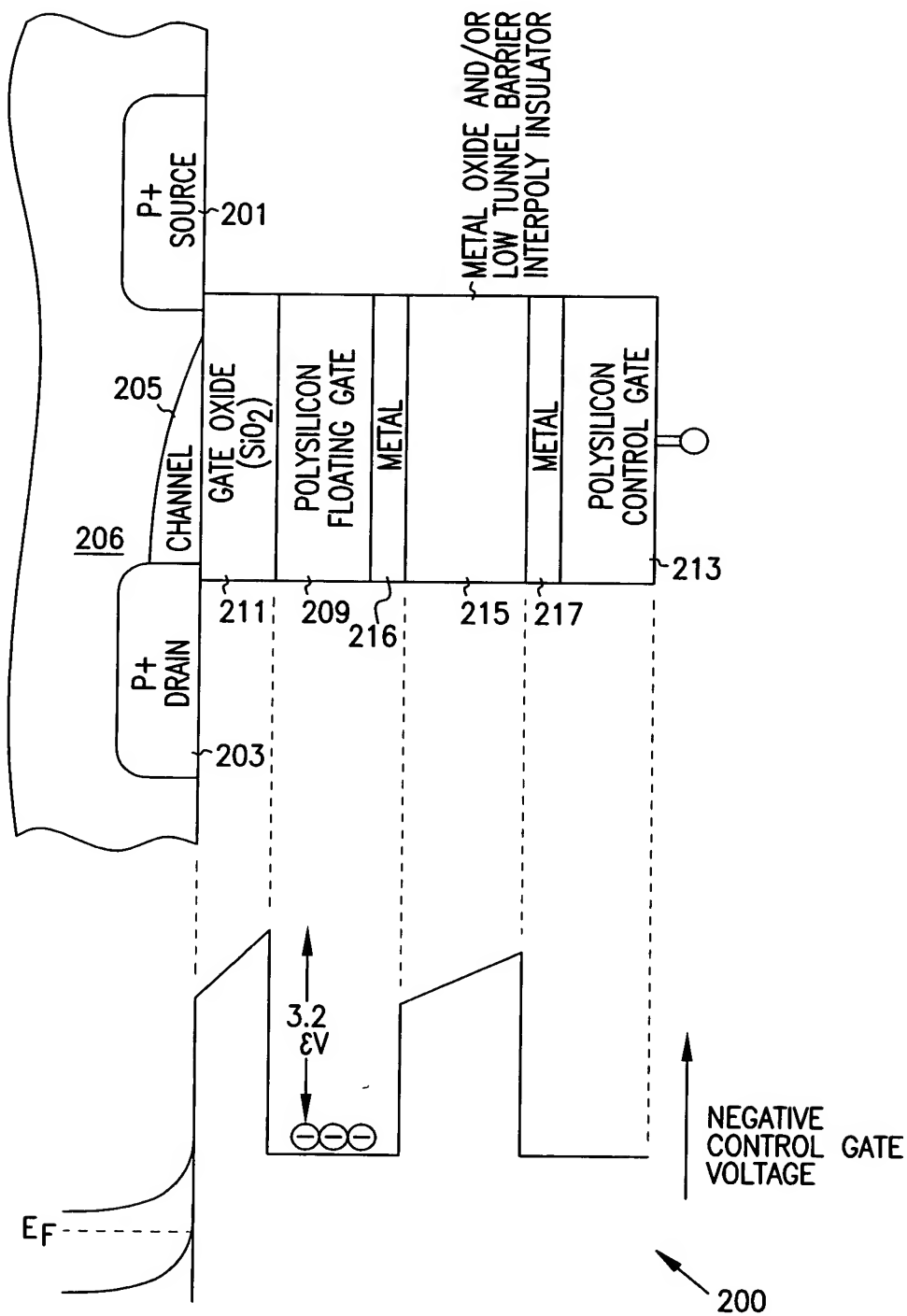


FIG. 2

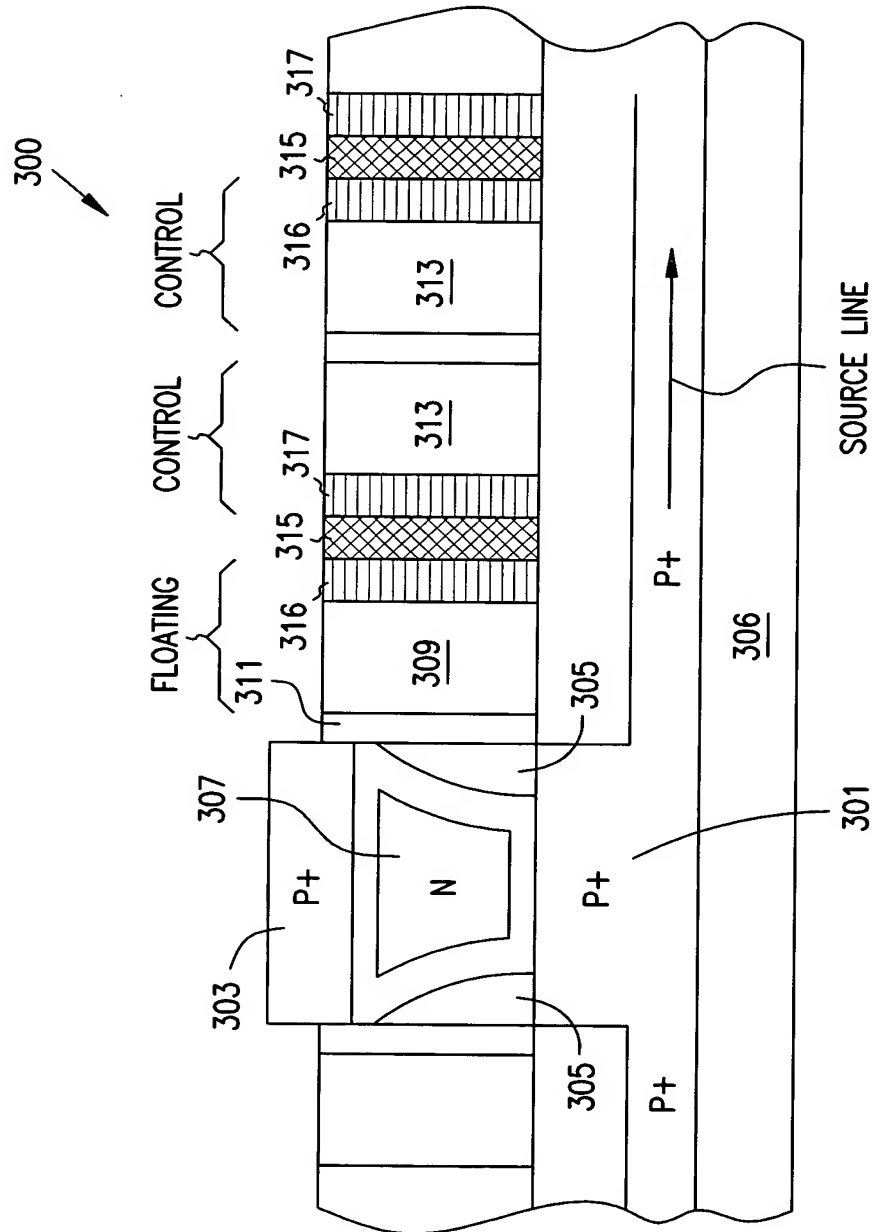


FIG. 3

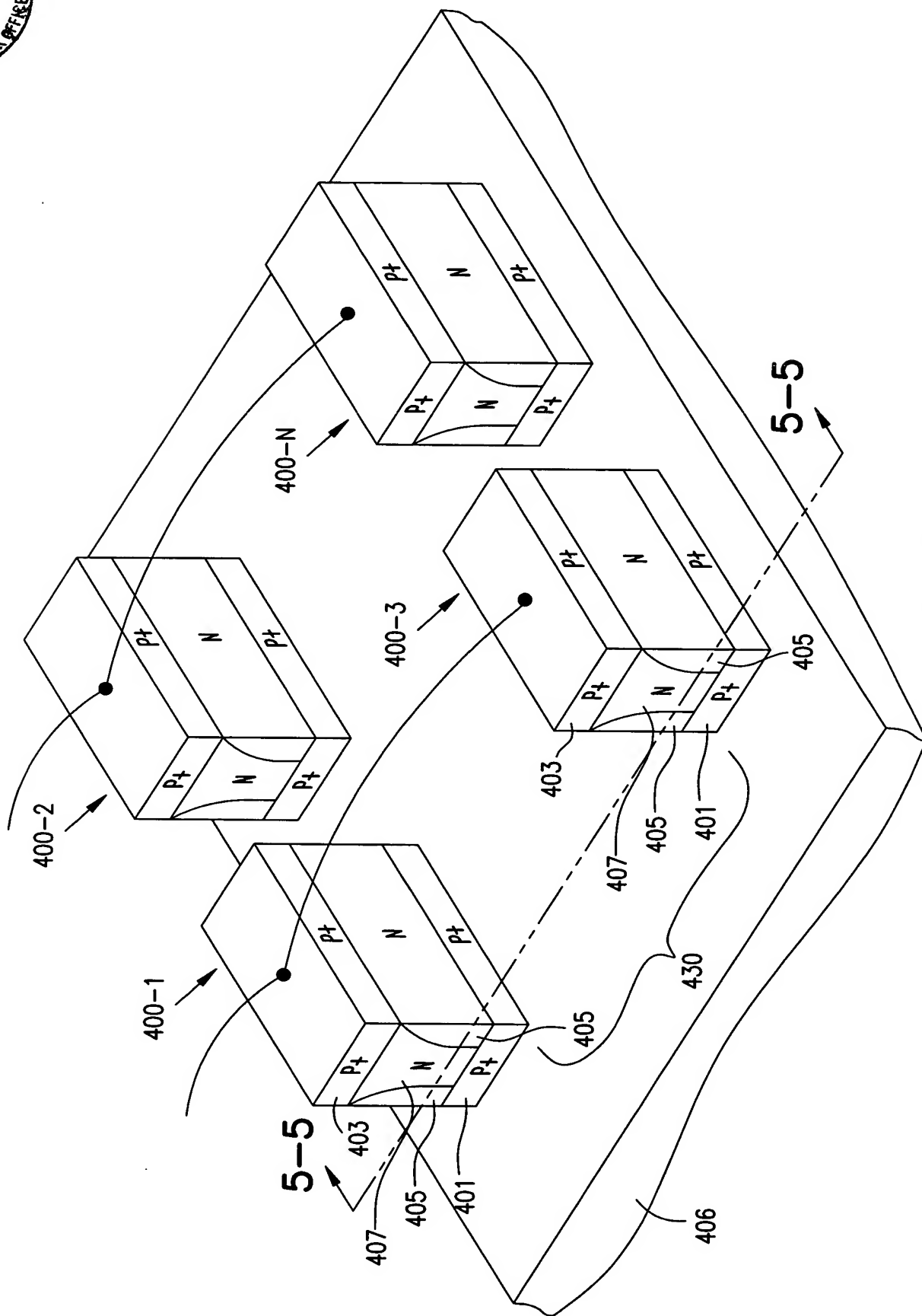


FIG. 4

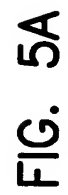


FIG. 5A

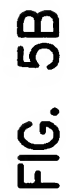


FIG. 5B



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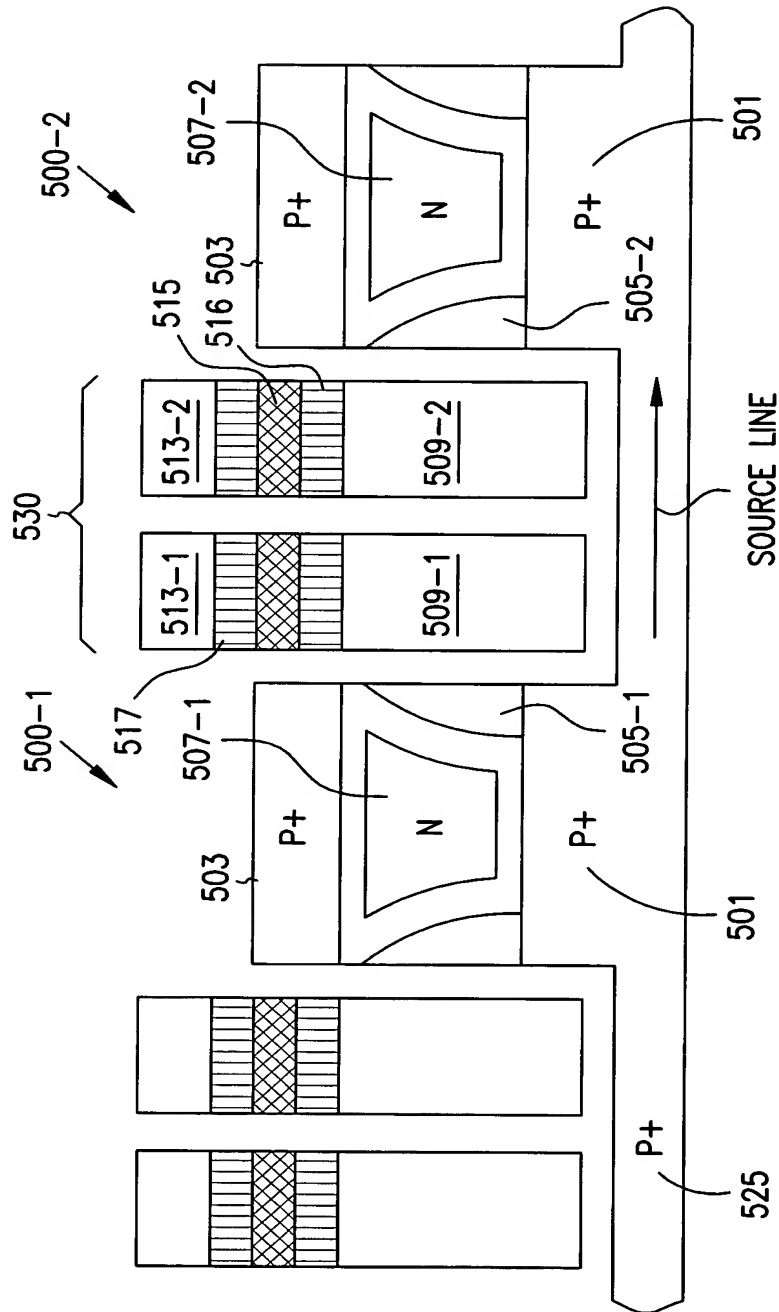
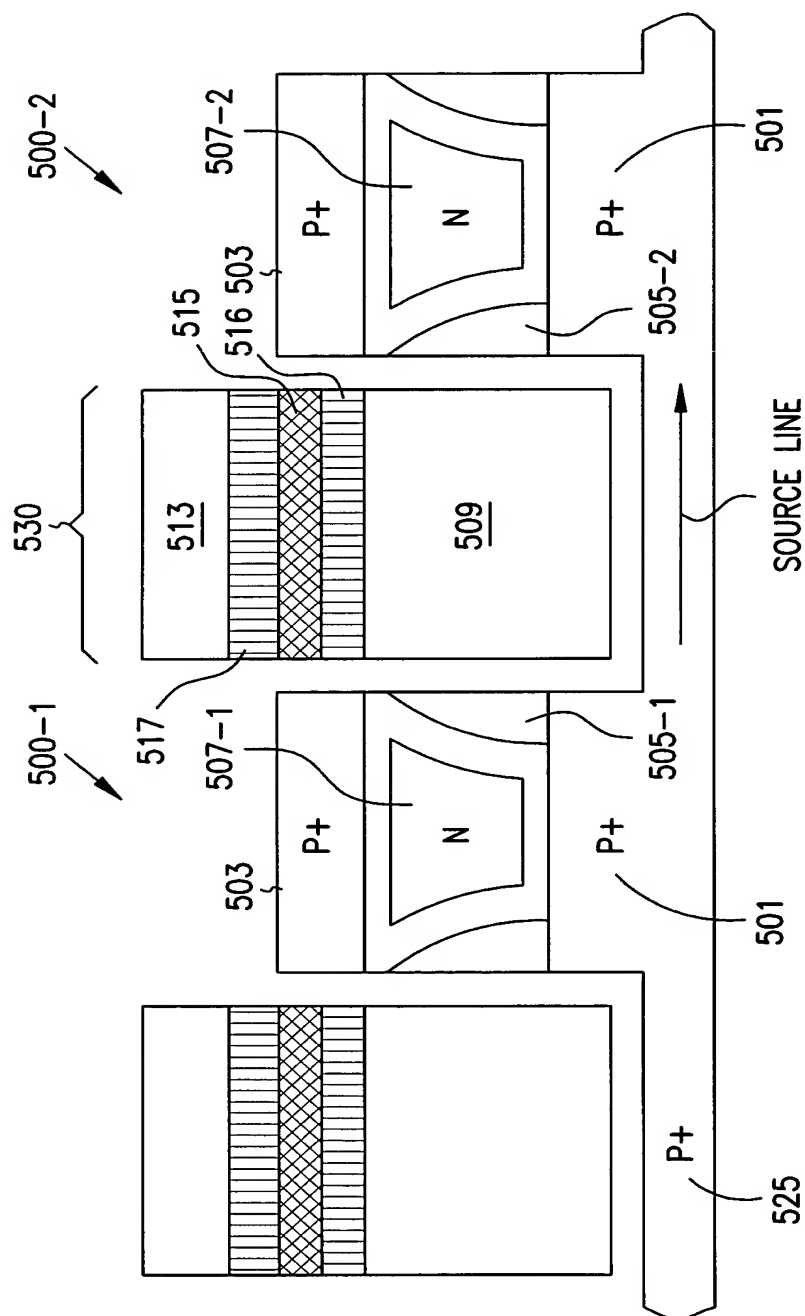


FIG. 5D



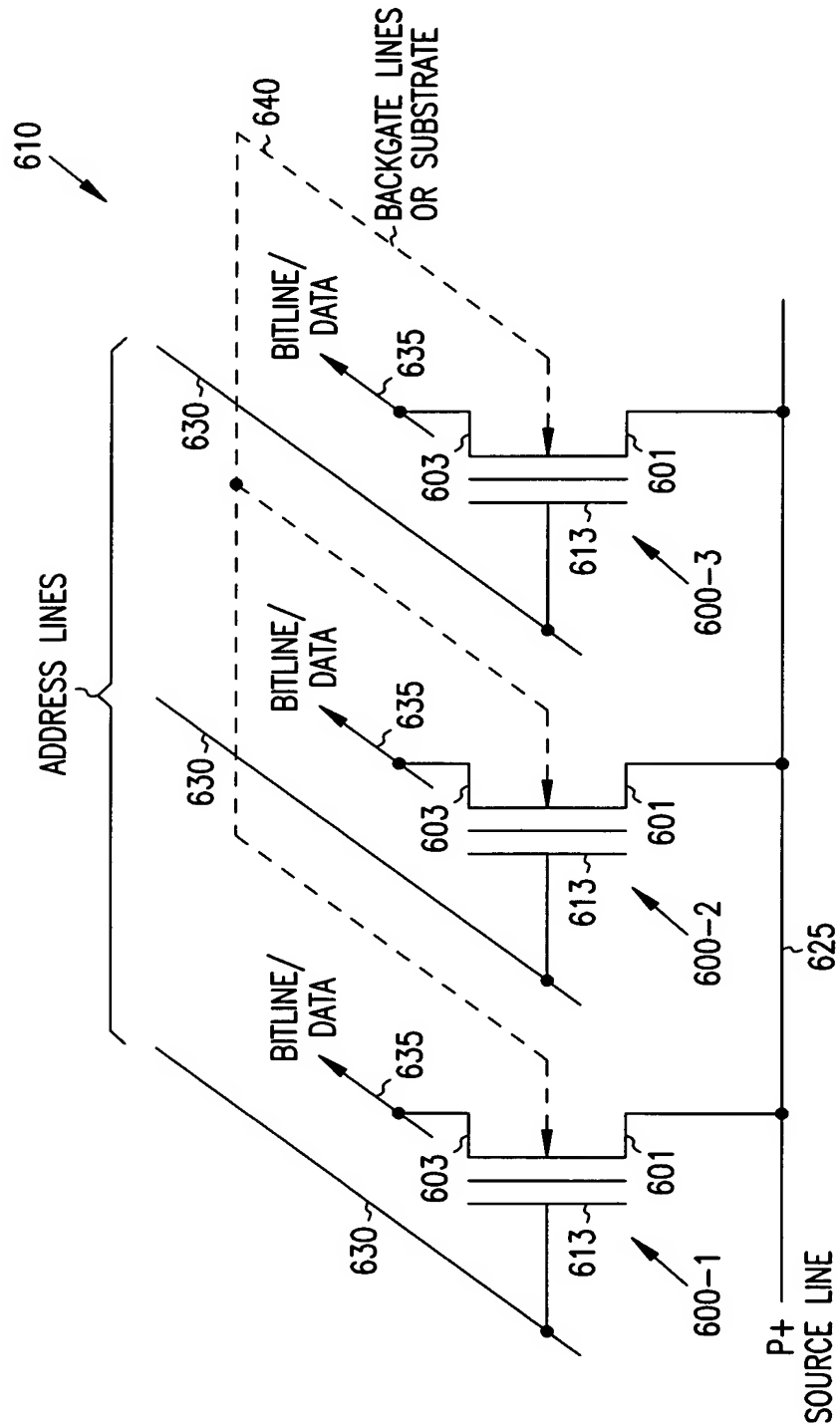


FIG. 6A

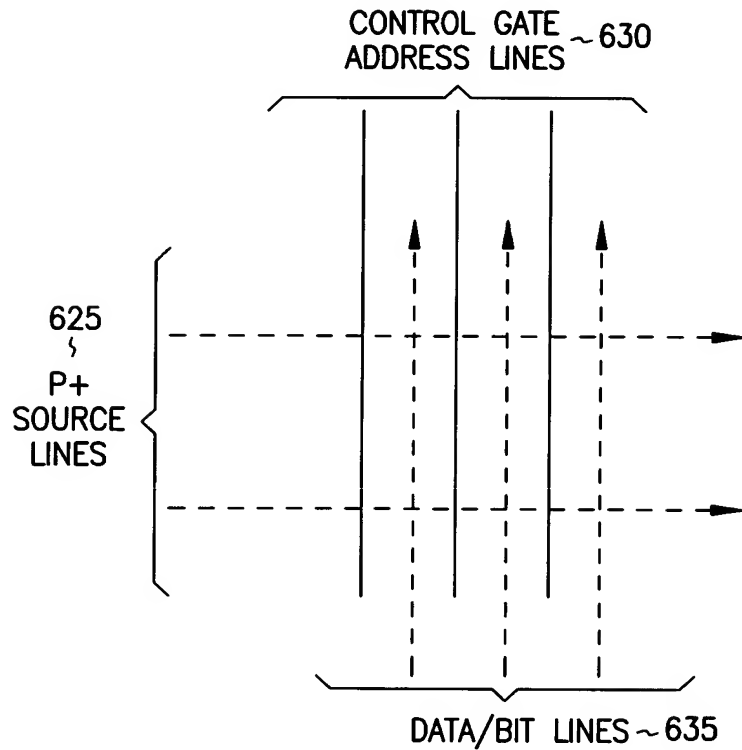


FIG. 6B

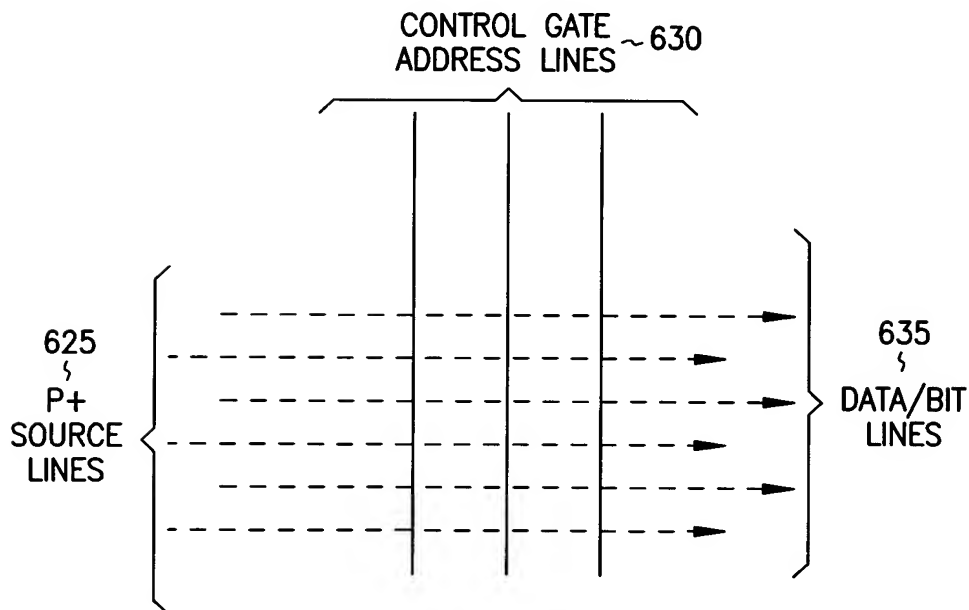


FIG. 6C

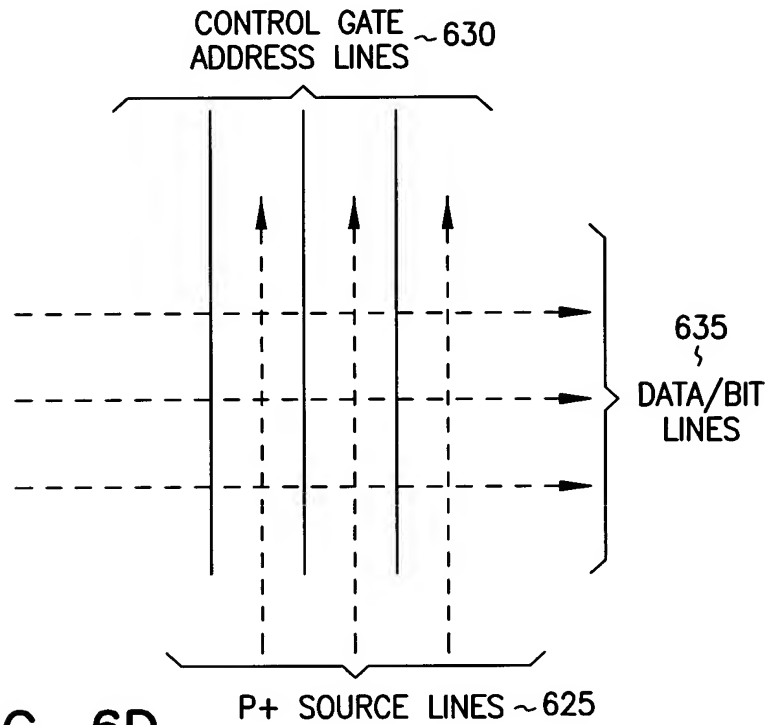


FIG. 6D

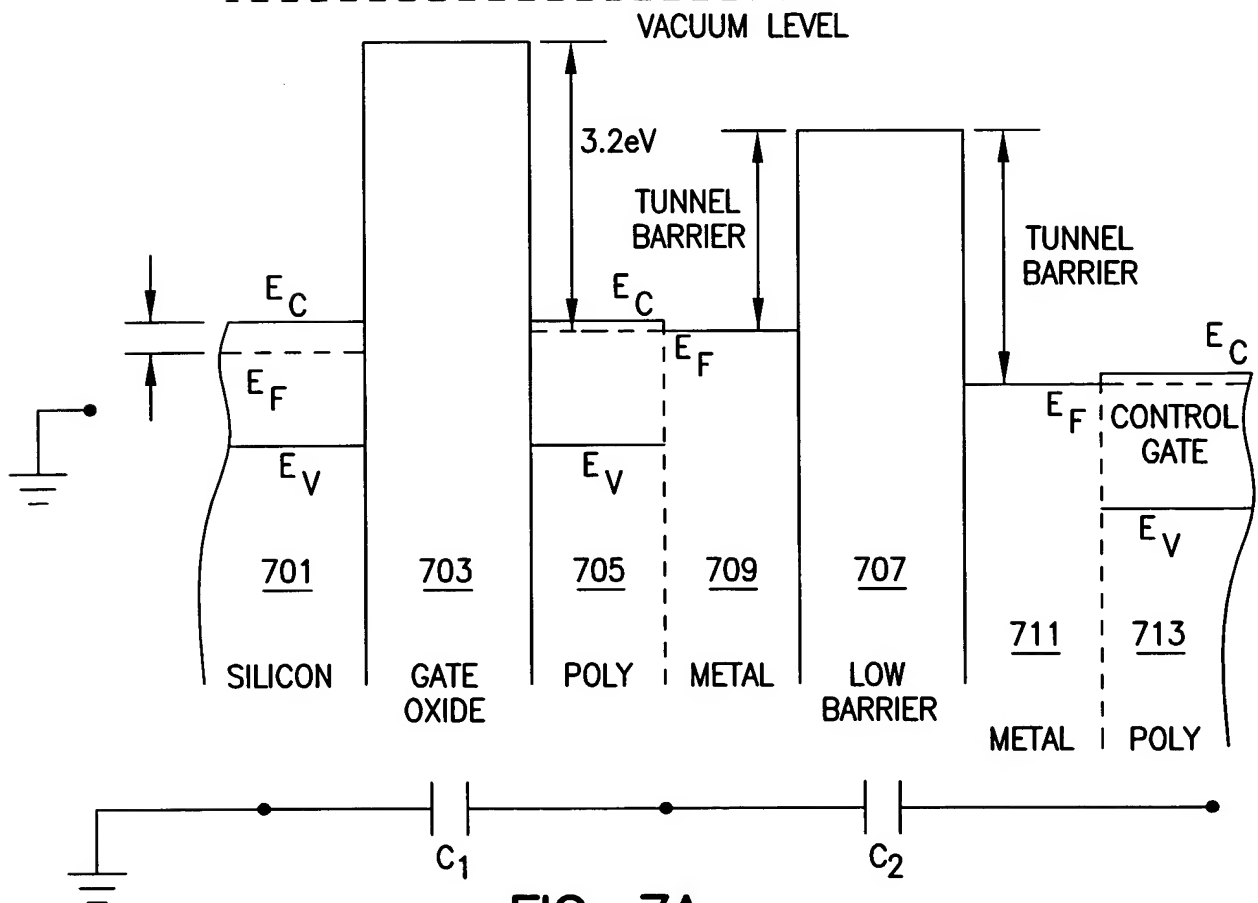


FIG. 7A

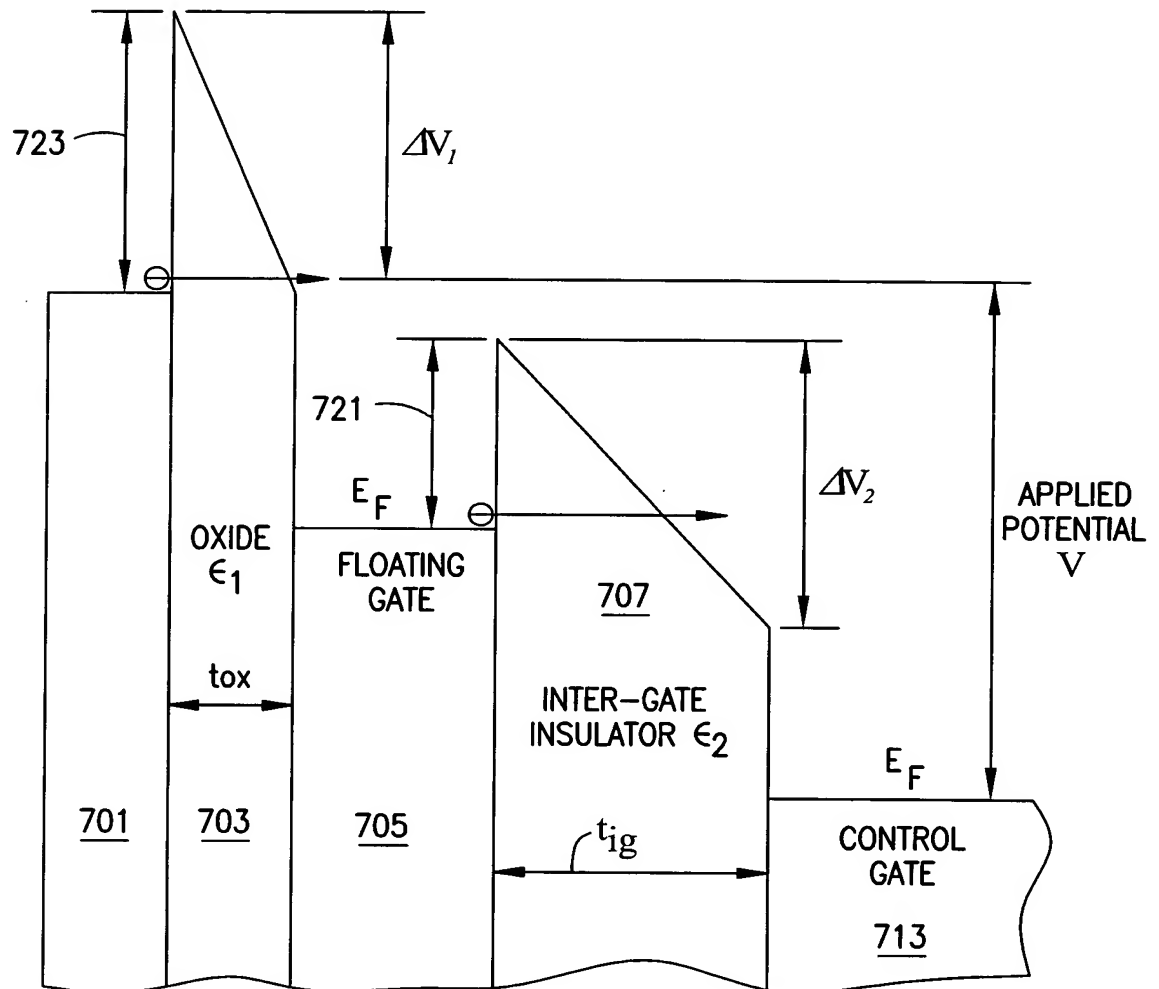


FIG. 7B



TITLE: PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND
ASYMMETRICAL TUNNEL BARRIERS
INVENTORS NAME: Leonard Forbes et al.
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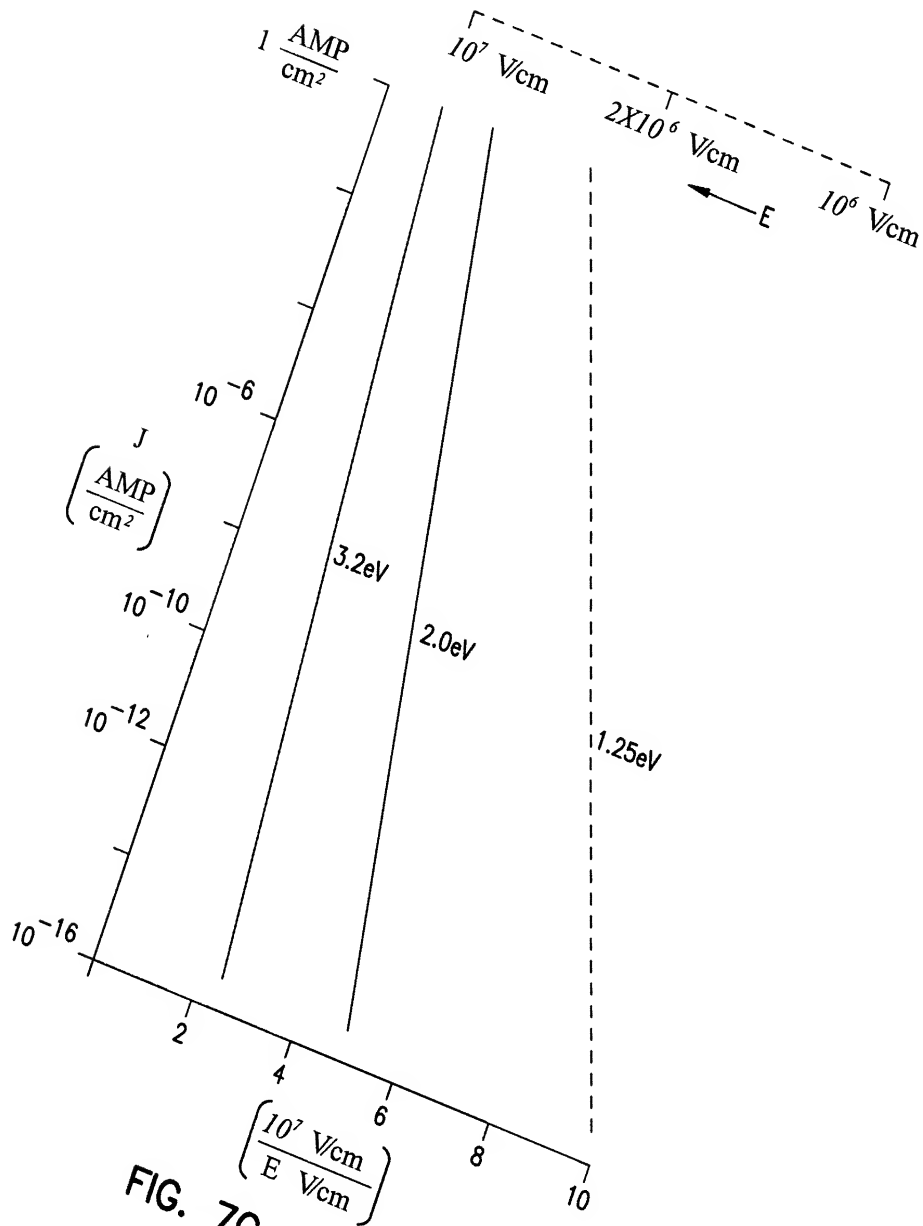


FIG. 7C

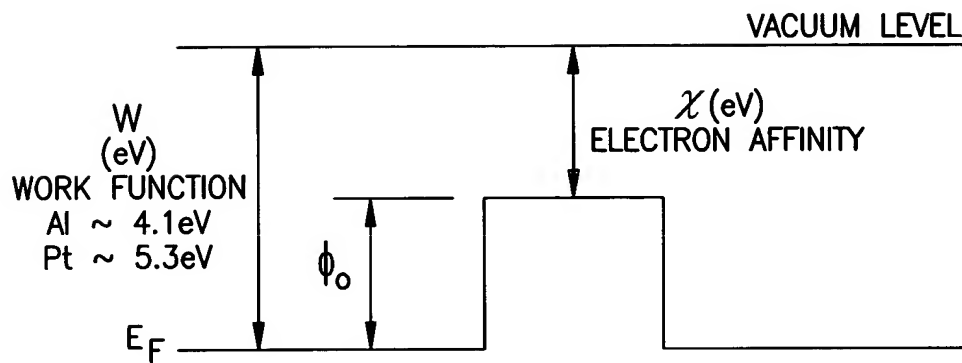
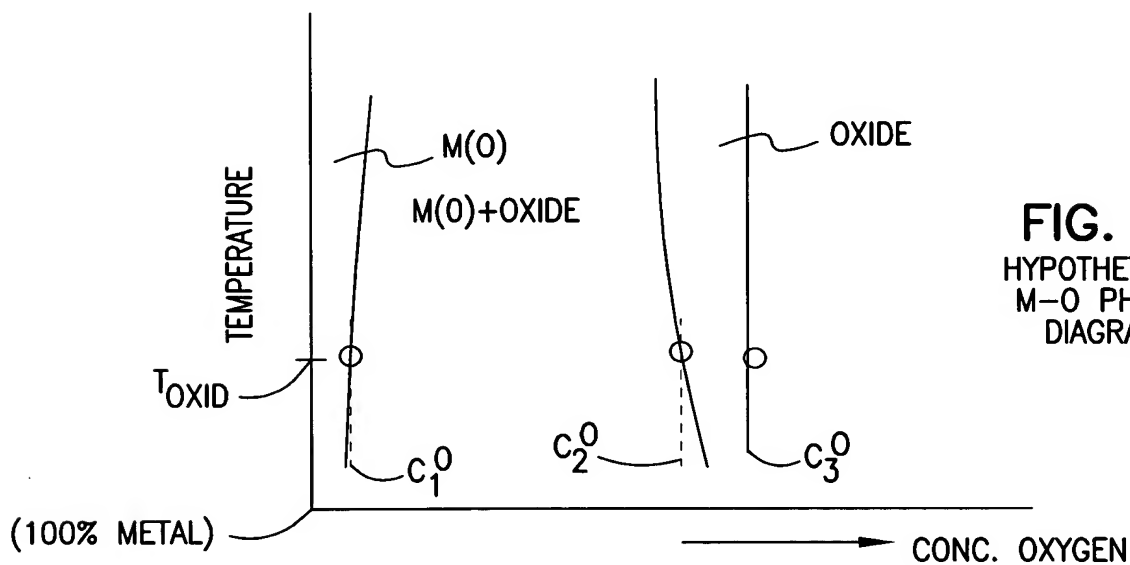
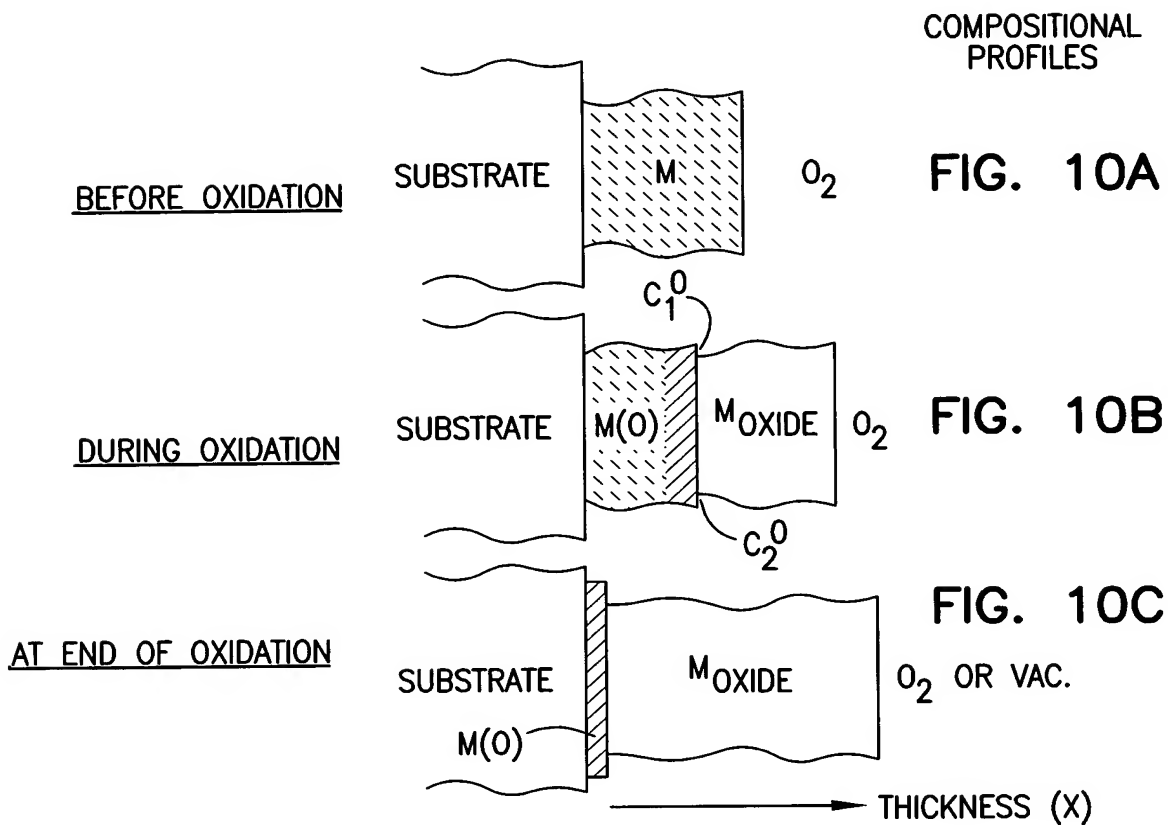


FIG. 8





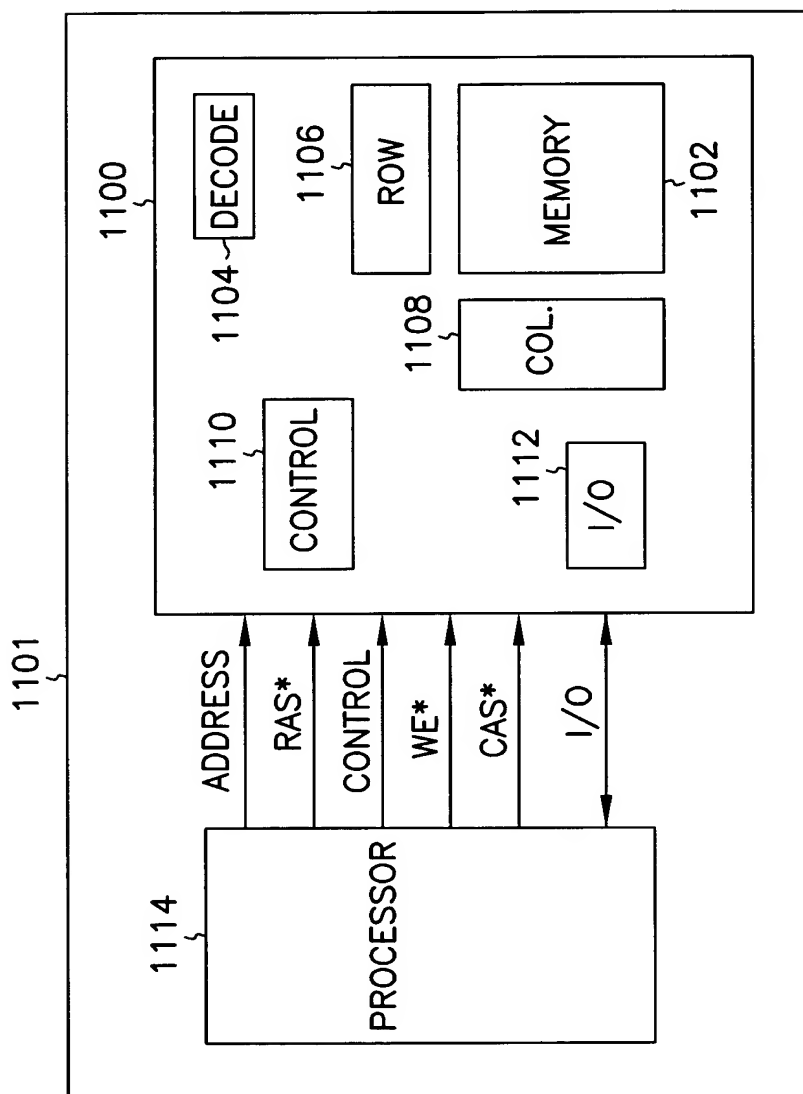


FIG. 11